Agenda

- Patent Policy:
  - The meeting is an official IEEE ad hoc. Please review the patent policy at the following site prior to the meeting. http://www.ieee802.org/3/patent.html
- Chip-Module Draft Baseline
  - SR & FEC
- Chip-Chip Discussion

Minutes

- Attendees: Daniel Dove, Pete Anslow, Kapil Shrikhande, Mike Dudek, Ali Ghiasi, John Petrilla, Wheling Cheng, Piers Dawe, Derek Cassidy, Richard Mellitz, Ted Sprague, Greg Lecheminant, Rick Rabinovich, Charles Moore, Scott Irwin, Tom Palkert, Phil McClay
- Reviewed Patent Policy
- Chip to Module
  - Discussion around FEC in relation to SR
    - Action for group to draw where FEC will reside in stack and location relative to CAUI (future presentation)
    - Current baseline assumes FEC doesn't increase bit rate, and FEC is not required to close CAUI4 link
    - Potential to have informative annex if CAUI extension is needed
  - Discussion around BER used for jitter spec
    - Range of potential solutions (VSR numbers at 1E-15, VSR numbers scaled to 1E-12, keep absolute VSR number but specify at 1E-12…)
  - Request to plot return loss comparisons (Tom has agreed to include in his presentation)
- Chip to chip
  - Reviewed Ali's chip-chip presentation for San Antonio
    - Discusses potential for a engineered chip-chip budget (up to 15dB) for higher loss budgets without FEC & MTTFPA issue